thereof. As shown, a substrate **12**, for example of P-type conductivity, has a well **14** of the same conductivity type as that of the substrate **12**. High concentration diffusion regions **16** and **126** of the same conductivity type as that of the substrate **12** and high concentration diffusion regions **18** and **124** of the opposite conductivity type (for example N-type) are formed in the well **14**, and the high concentration diffusion regions **126** and **124** are separated by a distance D. The high concentration diffusion region **16** and the high concentration diffusion regions **18**, **124** and **126** are separated by a field oxide (FOX) **45**. A gate **44** comprising a polysilicon layer **48** is spaced with a gate oxide **50** from a channel between the high concentration diffusion regions **18** and **124**. An insulator **24** covers the gate **44**, and contact windows **11**, **13** and **15** are formed in the insulator **24** for the high concentration diffusion regions **16**, **18** and **124**, respectively. A conductive layer **26** is electrically connected to the high concentration diffusion regions **16** and **18** in the contact windows **11** and **13**, so that the high concentration diffusion regions **16** and **18** are electrically connected to each other. A conductive layer **46** is electrically connected to the high concentration diffusion region **124** in the contact window **15**. The gate **44** and the high concentration diffusion regions **18** and **124** constitute a NMOS **150**. A diode **140** is present between the high concentration diffusion region **124** and the well **14**, and a diode **142** is present between the high concentration regions **124** and **126**. The high concentration diffusion regions **18** and **124** and the well **14** constitute a L-NPN BJT **136**, and resistor **138** is referred to the substrate resistor. During operation, the conductive layers **26** and **46** are electrically connected to ground and a pad **31**, respectively. When the pad **31** suffers an ESD event, along with the rising voltage, the diode **142** breaks down first since its breakdown voltage is lower than that of the diode **140**. The breakdown current flows through the resistor **138** to pump the substrate voltage, and thereby the BJT **136** is turned on to release the ESD current from the pad **31**. Similarly, in this embodiment, by altering the distance D, the breakdown voltage of the ESD protection device **146** is adjusted so as to protect the core circuit of the IC from damages effectively.

[0040] FIG. **20** shows an ESD protection device **152** for a BJT process application, and FIG. **21** is an equivalent circuit **156** thereof. As shown, a substrate **60**, for example of P-type conductivity, has a buried diffusion layer **86** of the opposite conductivity type (for example N-type). An epitaxial layer **62** of the conductivity type opposite to that of the substrate **60** covers the buried diffusion layer **86**. A diffusion region **80** of the same conductivity type as that of the substrate **60** and a diffusion region **84** of the conductivity type opposite to that of the substrate **60** are formed in the epitaxial layer **62**, and a diffusion region **82** of the conductivity type opposite to that of the substrate **60** is formed in the diffusion region **80**. A diffusion region **154** of the conductivity type opposite to that of the substrate **60** extends from the diffusion region **84** to a portion of the epitaxial layer **62** between the diffusion regions **80** and **84**. The above-mentioned structures are isolated into an independent unit by isolation diffusion regions **68** and **78** of the same conductivity type as that of the substrate **60**. A conductive layer **116** is electrically connected to the diffusion region **80**, a conductive layer **118** is electrically connected to the diffusion region **82**, and a conductive layer **120** is electrically connected to the diffusion region **154**. An insulator **88** covers a portion of each of the conductive layers **116**, **118** and **120**. The diffusion regions **82** and **80** and the epitaxial layer **62** constitute a V-NPN BJT **164**, a diode **158** is present between the diffusion region **80** and the epitaxial layer **62**, a diode **160** is present between the diffusion regions **80** and **154**, and resistor **162** is referred to the substrate resistor. The diffusion region **84** is the collector of the BJT **164**, the diffusion region **80** is the base, the diffusion region **82** is the emitter, the epitaxial layer **62** is used to increase the endurable voltage of the BJT **164**, and the doped concentration of the diffusion region **154** is higher than that of the diffusion region **84** to act as a contact area. In this embodiment, the conductive layer **116** is the base (B) of the BJT **164**, the conductive layer **118** is the emitter (E) of the BJT **164**, and the conductive layer **120** is the collector (C) of the BJT **164**. Similarly, when the pad **104** suffers an ESD event, along with the rising voltage, the diode **160** breaks down first since its breakdown voltage is lower than that of the diode **158**. The breakdown current flows through the resistor **160** to pump the substrate voltage, and thereby the BJT **164** is turned on to release the ESD current from the pad **31**. Similarly, in this embodiment, by altering the distance between the diffusion regions **80** and **154**, the breakdown voltage of the ESD protection device **152** is adjusted so as to protect the core circuit of the IC from damages effectively.

[0041] FIG. **22** shows an ESD protection device **200** for a HV-CMOS device. A substrate **202**, for example of P-type conductivity, has a well **204** of the conductivity type opposite to that of the substrate **202** and a well **206** of the same conductivity type as that of the substrate **202**. A high concentration diffusion region **208** of the conductivity type opposite to that of the substrate **202** is formed in the well **204**, and a high concentration diffusion region **210** of the same conductivity type as that of the substrate **202** is formed in the well **206**. An insulator **212** covers the substrate **202**, and contact windows **207** and **209** are formed in the insulator **212** for the high concentration diffusion regions **208** and **210**, respectively. Conductive layers **214** and **216** are electrically connected to the high concentration diffusion regions **208** and **210** in the contact windows **207** and **209**, respectively. The above-mentioned structures are isolated into an independent unit by a field oxide **205**. The region **218** forms a clamping diode. By adjusting the distance between the high concentration diffusion region **208** and the well **206** and the distance between the high concentration diffusion region **210** and the well **204** to adjust the distance between the high concentration diffusion regions **208** and **210**, the breakdown voltage of the clamping diode is between the power source voltage VCC and the breakdown voltage of the HV-CMOS device. When an ESD event occurs, due to the breakdown voltage of the clamping diode lower than that of the HV-CMOS device, the clamping diode breaks down earlier than the HV-CMOS device, and since the breakdown voltage of the clamping diode is higher than the power source voltage VCC, the power of the HV-CMOS device will not be short to ground. In other embodiments, by adjusting the distance between the high concentration diffusion region **208** and the well **206** or the distance between the high concentration diffusion region **210** and the well **204** to adjust the distance between the high concentration diffusion regions **208** and **210**, the breakdown voltage of the clamping diode is between the power source voltage VCC and the breakdown voltage of the HV-CMOS device. FIG. **23** shows a relationship of the distance between the high concentration diffusion region **208** and the well **206** and the breakdown voltage.